a barrier material (18) lining the walls of the via;

a seed layer overlying the barrier material and lining the walls of the via (Col. 4, lines 21-24); and

a conducting material (20) directly contacting the exposed surface of the circuit device.

Regarding claim 13, Obeng et al. teaches an integrated circuit, wherein the circuit device is an interconnected line.

Regarding claim 14, Obeng et al. teaches an integrated circuit, wherein the conductive material is copper.

Regarding claims 15 and 17 Obeng et al. does not explicitly teach an integrated circuit, wherein the barrier material can be etched in the presence of the seed material. Obeng et al. teaches an integrated circuit, wherein the barrier material and seed material comprise different materials that would have inherently used different etch chemistries/rates, thus the barrier material could have been etched selectively in the presence of the seed material. [Emphasis added]

Claim 12

Applicant submits that independent claim 12 is not anticipated by Obeng for at least the reason that Obeng does not teach, suggest or describe "a conductive material directly contacting the surface of the circuit device," as claimed in independent claim 12. It is axiomatic that to be anticipated, every element of claim 12 must be disclosed within a single reference. The Patent Office relies upon conductive material (20) of Obeng to address the features quoted above of claim 12. Obeng describes forming copper interconnects in ULSI circuits by lining circuit trenches and vias with a self-assembling organic film barrier layer, depositing a seed layer over the barrier layer, and then capping the seed layer with a thick copper film. For instance, at col. 4, lines 21-24, Obeng states:

> A thin diffusion barrier/adhesion promoter film 18 may the be deposited, which again may be a self assembling organic film, followed by the deposition of a copper seed layer which is then capped with a thick copper film 20 by known techniques to give rise to the structure shown in FIG. 1(b). [Emphasis added]

Obeng then describes polishing the thick copper layer down to the dielectric layer, and then covering, the exposed copper layer and dielectric layer with another layer of self-assembling film. Obeng goes on to say that the above steps can be repeated to form a device having multi-level interconnects. For example, at col. 4, lines 33-35 Obeng states:

> The above steps may then be repeated as required to form a device having multilevel interconnections as shown in **FIG. 1(*d*)**.

However, the Patent Office has not identified and the Applicant has been unable to find any description in Obeng of removing either barrier film 18 or the copper seed layer deposited in the via. Therefore, in any instance of capping a via with thick copper film 20, Obeng teaches thick copper film 20 capped over both diffusion film 18 and a copper seed layer.

In contrast to Obeng, Applicant's claim 12 includes "a conductive material directly contacting the surface of the circuit device." Therefore, the direct contact required in claim 12 is distinct from the capping of barrier film 18 and copper seed layer between thick copper film 20 and a circuit device below "by known techniques" as described in Obeng.

Furthermore, in the Final Office Action, the Patent Office addresses the Applicant's arguments filed June 3, 2002 that Obeng shows a diffusion barrier/adhesion promoter film 18, as well as a dark line copper seed layer between thick copper film 20 and underlying silicon substrate 12. The Patent Office finds that argument unpersuasive stating:

> It is likely that the applicant is correct in that the dark line may represent the [cooper] seed layer and it is between the circuit device and the silicon. However, the circuit device that is formed in the insulative portion of the substrate is in direct contact with the conductive structure formed above it. This is further evidenced in the above cited passage, where Obeng et al. goes on to say, "The remaining exposed copper 22..." (emphasis added). Therefore it can be seen that Obeng et al. teaches a conductive material (20) directly connected to a circuit device, said device being an interconnect structure, which is exactly what is claimed in the instant application. [Emphasis added]

Thus, the Patent Office admits that either: (1) due to the seed layer, thick copper film 20 is not in direct contact with underlying silicon substrate 12; or (2) that it is unclear due to the seed layer whether or not thick copper film 20 is in direct contact with underlying silicon substrate 12.

In the first admission instance above, the Patent Office's rebuttal that "the circuit device that is formed in the insulative portion of the substrate is in direct contact with

the conductive structure formed above it... it can be seen that Obeng et al. teaches a conductive material (20) directly connected to a circuit device, said device being an interconnect structure" cannot be correct. [Emphasis added] This is because, as noted above, Obeng only describes thick copper film 20 capping the seed layer and the barrier film. Thus, the formation of the conductive material 20 on the left side of Figure 1D of Obeng cited by the Patent Office above, requires that the interconnect structure of the insulative portion substrate be formed by repeating the steps that the Patent Office admits includes leaving a copper seed layer between the conductive material 20 and the structure below it. Specifically, as noted above by the Applicant, the structures in Figure 1D of Obeng formed over the structures of Figure 1C are formed by repeating the steps described at col. 4, lines 21-24 of Obeng and shown in Figures 1A-1C. Thus it is clear that the dark line copper seed layer shown in Figure 1C must also exist between conductive material 20 and the interconnect structure circuit device that is formed in the insulative portion of the substrate in Figure 1D. In addition, Applicant asserts that the line shown in Figure 1D of Obeng, between second copper layer 20 and interconnect structure below is a seed layer between copper layer 20 and the underlying interconnect structure of Figure 1D. Therefore, Obeng does not describe a conductive material directly contacting the surface of a circuit device.

Furthermore, Applicant asserts that Figures 1C and 1D of Obeng are inconsistent with respect to the thick copper film 20 capping as described in Figure 1B and in the specification of Obeng. For example, in Figure 1B and col. 4, lines 21-24 of Obeng show and describe diffusion barrier 18 and a copper seed layer in the via between thick copper film 20 and underlying silicon substrate 12. However, the Patent Office has not identified and the Applicant is unable to find any teaching or description in Obeng of removing either the barrier layer 18 or the copper seed layer which are clearly shown in Figure 1B existing in the via between thick copper film 20 and silicon substrate 12.

Contrary to Figure 1B of Obeng, in Figure 1C diffusion barrier 18 appears to be omitted in the figure via between copper layer 22 and substrate 12. Moreover, on the left side of Figure 1D, second copper layer 20 formed over interconnect structure 20 using the same steps to form the structures in Figures 1B and 1C also omits barrier film 18 and appears with a thinner line between the copper layers. Particularly, the

formation of this second copper layer requires deposition of dielectric layer 10, etching of the trench and via, deposition of barrier film 18, and deposition of a copper seed layer as described in col. 4, lines 20-24, and shown in Figure 1B of Obeng. Therefore, since the Patent Office has not identified, and the Applicant is unable to find any teaching or suggestion of removal of the seed layer or barrier layer, those layers should exist in Figures 1C and 1D between copper layer 20 and the interconnect structure below, as cited by the Patent Office. For this reason, the Applicant asserts that Figures 1C and 1D of Obeng are inconsistent with the description provided in col. 4, lines 11-35, and Figure 1B of Obeng, and that Figures 1C and 1D therefore do not describe an enabled teaching of Obeng that can be cited as a reference by the Patent Office in accordance with MPEP §2121. This contention is further supported by the Patent Office's admission that "it is likely that the applicant is correct that the dark line may represent the copper seed layer and it is between the circuit device and the silicon." [Emphasis added] Here, it is clear, and the Patent Office should agree, that Figures 1B, 1C and 1D of Obeng are inconsistent with regard to whether or not thick copper film 20 is in direct contact with any underlying substrate or interconnect structure.

More particularly, as practiced in the art, "known techniques" of capping a circuit device with thick copper film 20 include capping a barrier layer and a seed layer between the thick copper film 20 and any structure below. Thus, Applicant respectfully requests that the Patent Office withdraw the rejection of independent claim 16 under 35 U.S.C. §102(e) as anticipated by Obeng, because: (1) Obeng does not describe a conductive material in direct contact with the surface of circuitry below; (2) the portion of Obeng cited by the Patent Office is inconsistent with the related descriptions of Obeng; and 3) the portion of Obeng cited by the Patent Office is not enabled.

Claim 16

Applicant submits that independent claim 16 is not anticipated by Obeng for at least the reason that Obeng does not teach, suggest or describe a conductive material in a via having a seed layer and a barrier material formed so as to expose a circuit device at an end of the via. It is axiomatic that to be anticipated, every element of claim 16 must also be disclosed within Obeng. However, as described above, for a conductive material directly contacting the surface of a circuit device as claimed in claim 12, the

Patent Office has not identified and the Applicant is unable to find any teaching or suggestion in Obeng of a conductive material in a via having a seed layer and barrier material formed to expose the circuit device at an end of the via. Therefore, these limitations of claim 16 are distinct from the known techniques of capping a barrier film and copper seed layer of Obeng. Thus, Applicant respectfully requests that the Patent Office withdraw the rejection of independent claim 16 under 35 U.S.C. §102(e) as anticipated by Obeng.

Claims 15 and 17

Applicant submits that dependent claims 15 and 17 are further not anticipated by Obeng for at least the reason that Obeng does not teach, suggest or describe a barrier layer with etched characteristics so that the barrier material can be selectively etched in the presence of the seed material.

Applicant's dependent claims 15 and 17 each include "wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material." It is axiomatic that for these claims to be anticipated Obeng must teach these limitations in addition to those of the base claims. To address these limitations, the Patent Office states on page 3 of the Final Office Action, "Obeng et al. teaches an integrated an integrated circuit, wherein the barrier material and seed material comprise different materials that would have inherently used different etch chemistries/rates." In order for a limitation to be inherent, it must necessarily flow from the teachings of the prior art. Thus, the fact that a feature may occur in a reference is not sufficient to establish its inherency. For example, although the barrier material and seed material in Obeng may be different materials, it does not necessarily flow that those materials have different etch chemistries or rates, because according to the typical damascene process used in Obeng (Obeng, col. 3, line 64), the barrier layer is a refractory material which inhibits the diffusion of the interconnect material into the dielectric, and the seed material lines the barrier material so that the interconnect material will form properly within the via and trench. However, although the barrier material and seed material are different materials, they may have the same etch rate, similar etch rates, the seed material may be more susceptible to etching than the barrier material such that the barrier material cannot be selectively etched in the

presence of the seed material. Therefore, it does not necessarily flow that the barrier material and seed material of Obeng use different etch chemistries/rates. For this additional reason, Applicant respectfully requests that the Patent Office withdraw the rejection of claims 15 and 17 under 35. U.S.C. §103(e) as anticipated by Obeng.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: October 23, 2002

Angelo J. Gaz, Reg. No.: 45,907

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office, BOX AF, Assistant Commissioner for Patents, Washington, D.C. 20231, on October 23, 2002.

Margaux Rodriguez *October 23, 2002*